The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-20. (Canceled)

21. (Previously Presented) An active matrix display device having a pixel portion and a driver circuit portion, said driver circuit portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and a part of the driver circuit portion;

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V{\cdot}sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V{\cdot}sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the driver circuit portion are formed by a same process simultaneously.

22. (Previously Presented) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and the shift register; and

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V{\cdot}sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V{\cdot}sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the shift register are formed by a same process simultaneously.

23. (Previously Presented) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter; and

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the inverter are formed by a same process simultaneously .

24. (Previously Presented) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter; and

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the clocked inverter are formed by a same process simultaneously.

25. (Previously Presented) An active matrix display device having a pixel portion and a driver circuit portion, said driver circuit portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and a part of the driver circuit portion; and

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V{\cdot}sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V{\cdot}sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein a laser Raman spectroscopy of the crystalline semiconductor islands of the thin film transistors of the pixel portion and the driver circuit portion exhibits a peak shifted to a lower frequency side as compared with a peak of single crystal silicon.

26. (Previously Presented) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel

and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and in the shift register; and

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the shift register are formed by a same process simultaneously.

27. (Previously Presented) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter; and

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 cm2/V·sec or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 cm2/V·sec or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the inverter are formed by a same process simultaneously .

28. (Previously Presented) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter; and

a pixel electrode formed over the leveling film,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V{\cdot}sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V{\cdot}sec$ or more, wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the clocked inverter are formed by a same process simultaneously.

29. (Previously Presented) An active matrix display device having a pixel portion and a driver circuit portion, said driver circuit portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said p-channel and n-channel thin film transistors in both of the pixel portion and a part of the driver circuit portion; and

a pixel electrode formed over the leveling film,

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

30. (Previously Presented) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and the shift register; and

a pixel electrode formed over the leveling film,

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

31. (Previously Presented) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter; and

a pixel electrode formed over the leveling film,

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

32. (Previously Presented) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter; and

a pixel electrode formed over the leveling film,

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

33. (Previously Presented) A semiconductor device according to any one of claims 22-24, 26-28, and 30-32 wherein said semiconductor is silicon.

34. (Previously Presented) A semiconductor device according to any one of claims 22-24, 26-28, and 30-32 wherein said gate electrode comprises crystalline silicon doped with phosphorus.

35. (Previously Presented) A semiconductor device according to any one of claims 22-24, 26-28, and 30-32 wherein said gate electrode is a multilayer film of crystalline silicon doped with phosphorus and a metal film thereon, said metal comprising at least a material selected from the group consisting of Mo, W. $MoSi_2$, and Wsi_2.

36. (Previously Presented) A semiconductor device according to any one of claims 22-24, 26-28, and 30-32 wherein said semiconductor island comprises oxygen at a concentration not higher than $1x10^{19}$ cm^{-3}.

37. (Previously Presented) A semiconductor device according to any one of claims 22-24, and 30-32 wherein said crystalline semiconductor island exhibits a Raman peak shifted to a lower frequency side from 522 cm^{-1}.

38. (Previously Presented) A semiconductor device according to claim 34 wherein said phosphorus doped in said crystalline silicon is at a concentration of $1x10^{21}$ to $5x10^{21}$ cm^{-3}.

39. (Previously Presented) A semiconductor device according to any one of claims 22-24, 26-28, and 30-32 wherein said source and drain regions of n-channel thin film transistor are introduced with phosphorus at a dose of $1x10^{15}$ to $5x10^{15}$ cm^{-3}.

40. (Previously Presented) A semiconductor device according to any one of claims 22-24, 26-28, and 30-32 wherein said semiconductor island has a thickness of 500-5000 Å.

41. (Previously Presented) An active matrix display device including a pixel portion and a driver circuit portion comprising:

a plurality of pixel electrodes formed on an insulating surface;

a first plurality of thin film transistors being formed in the pixel portion on said insulating surface and being connected to said pixel electrodes;

a second plurality of thin film transistors being formed in the driver circuit portion on said insulating surface, said second plurality of thin film transistors including at least one pair of complementary p-channel and n-channel thin film transistors; and

a leveling film covering both of the first and second plurality of thin film transistors in the pixel portion and a part of the driver circuit portion, wherein said pixel electrodes are formed over the leveling film,

wherein said second plurality of thin film transistors in said driver circuit include channel semiconductor layers having at least one of an electron mobility 15 $cm^2/V \cdot sec$ or more and a hole mobility of 10 $cm^2/V \cdot sec$ or more, and

wherein each of said channel semiconductor layers has a thickness of 5000 Å or less.

42. (Canceled)

43. (Previously Presented) A device according to claim 41 wherein said semiconductor is silicon.

44. (Previously Presented) A device according to claim 41 wherein each of the first and second plurality of said thin film transistors comprises a gate electrode formed over said channel semiconductor layers having a gate insulating film therebetween.

45. (Previously Presented) A device according to claim 44 wherein said gate electrode comprises crystalline silicon doped with phosphorus.

46. (Previously Presented) A device according to claim 44 wherein said gate electrode is a multilayer film of crystalline silicon doped with phosphorus and a metal film thereon, said metal comprising at least a material selected from the group consisting of Mo, W, $MoSi_2$, and WSi_2.

47. (Previously Presented) A device according to claim 45 or 46 wherein said phosphorus doped in said crystalline silicon is at a concentration of $1x10^{21}$ to $5x10^{21}$ cm^{-3}.

48. (Previously Presented) A device according to claim 41 wherein said channel semiconductor layers exhibit a Raman peak shifted to a lower frequency side from 522 cm^{-1}.

49. (Previously Presented) A device according to any one of claims 21, 25, and 29 wherein said semiconductor is silicon.

50. (Previously Presented) A device according to any one of claims 21, 25, and 29 wherein said gate electrode comprises crystalline silicon doped with phosphorus.

51. (Previously Presented) A device according to any one of claims 21, 25, and 29 wherein said gate electrode is a multilayer film of crystalline silicon doped with phosphorus and a metal film thereon, said metal comprising at least a material selected from the group consisting of Mo, W, $MoSi_2$, and WSi_2.

52. (Previously Presented) A device according to any one of claims 21, 25, and 29 wherein said semiconductor island comprises oxygen at a concentration not higher than $1x10^{19}$ cm^{-3}.

53. (Previously Presented) A device according to any one of claims 21, and 29 wherein said crystalline semiconductor island exhibits a Raman peak shifted to a lower frequency side from 522 cm^{-1}.

54. (Previously Presented) A device according to claim 30 or 31 wherein said phosphorus doped in said crystalline silicon is at a concentration of $1x10^{21}$ to $5x10^{21}$ cm^{-3}.

55. (Previously Presented) A device according to any one of claims 21, 25, and 29 wherein said source and drain regions of n-channel thin film transistor are introduced with phosphorus at a dose of $1x10^5$ to $5x10^5$ cm^{-2}.

56. (Previously Presented) A device according to any one of claims 21, 25, and 29 wherein said semiconductor island has a thickness of 500-5000 Å.

57. (Previously Presented) A semiconductor device according to any one of claims 22-24, 26-28, and 30-32, wherein said leveling film comprises an organic resin.

58. (Previously Presented) A semiconductor device according to claim 57, wherein said organic resin is a transparent polyimide resin.

59. (Previously Presented) A device according to any one of claims 21, 25, 29, and 41, wherein said leveling film comprises an organic resin.

60. (Previously Presented) A device according to claim 59, wherein said organic resin is a transparent polyimide resin.

61. (Previously Presented) A semiconductor device according to any one of claims 22-24, 26-28, and 30-32, wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 200 $cm^2/V \cdot sec$ or less and said semiconductor island of n-channel thin film transistor has a electron mobility in the range of 300 $cm^2/V \cdot sec$ or less.

62. (Previously Presented) A device according to any one of claims 21, 25, and 29, wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 200 $cm^2/V \cdot sec$ or less and said semiconductor island of n-

channel thin film transistor has a electron mobility in the range of 300 $cm^2/V \cdot sec$ or less.

63. (Previously Presented) A device according to claim 41, wherein said second plurality of thin film transistors in said driver circuit include channel semiconductor layers having at least one of an electron mobility 300 $cm^2/V \cdot s$ or less and a hole mobility of 200 $cm^2/V \cdot s$ or less.

64. (Previously Presented) A semiconductor device according to any one of the claims 22-24, and 30-32, wherein said n-channel thin film transistor has an approximately same absolute value of a threshold voltage as said p-channel thin film transistor.

65. (Previously Presented) A device according to any one of the claims 21, 25, 29, wherein said n-channel thin film transistor has an approximately same absolute value of a threshold voltage as said p-channel thin film transistor.

66. (Previously Presented) A semiconductor device according to claim 35 wherein said phosphorus doped in said crystalline silicon is at a concentration of $1x10^{21}$ to $5x10^{21}$ cm^{-3}.

67. (Previously Presented) A device according to claim 22 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3}.

68. (Previously Presented) A device according to claim 23 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3}.

69. (Previously Presented) A device according to claim 24 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3}.

70. (Currently Amended) A device according to claim 25 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially the same [[the]] as an absolute value of a threshold voltage of said p-channel thin film transistor.

71. (Currently Amended) A device according to claim 26 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially the same [[the]] as an absolute value of a threshold voltage of said p-channel thin film transistor.

72. (Currently Amended) A device according to claim 27 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially the same [[the]] as an absolute value of a threshold voltage of said p-channel thin film transistor.

73. (Currently Amended) A device according to claim 28 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially the same [[the]] as an absolute value of a threshold voltage of said p-channel thin film transistor.

74. (Previously Presented) A device according to claim 29 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3}.

75. (Previously Presented) A device according to claim 30 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3}.

76. (Previously Presented) A device according to claim 31 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3}.

77. (Previously Presented) A device according to claim 32 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3}.

78. (Previously Presented) A device according to claim 41 wherein each of the channel semiconductor layers comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3}.

79. (Previously Presented) The active matrix display device according to claim 29 wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V{\cdot}sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V{\cdot}sec$ or more.

80. (Previously Presented) The active matrix display device according to claim 29 wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the driver circuit portion are formed by a same process simultaneously.

81. (Previously Presented) The active matrix display device according to claim 29 wherein a laser Raman spectroscopy of the crystalline semiconductor islands of the thin film transistors of the pixel portion and the driver circuit portion exhibits a peak shifted to a lower frequency side as compared with a peak of single crystal silicon.

82. (Previously Presented) The semiconductor device according to claim 30 wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V{\cdot}sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V{\cdot}sec$ or more.

83. (Previously Presented) The semiconductor device according to claim 30 wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the shift register are formed by a same process simultaneously.

84. (Previously Presented) The semiconductor device according to claim 30 wherein a laser Raman spectroscopy of the crystalline semiconductor islands of the thin film transistors of the pixel portion and the shift register exhibits a peak shifted to a lower frequency side as compared with a peak of single crystal silicon.

85. (Previously Presented) The semiconductor device according to claim 31 wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V{\cdot}sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V{\cdot}sec$ or more.

86. (Previously Presented) The semiconductor device according to claim 31 wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the inverter are formed by a same process simultaneously.

87. (Previously Presented) The semiconductor device according to claim 31 wherein a laser Raman spectroscopy of the crystalline semiconductor islands of the thin film transistors of the pixel portion and the inverter exhibits a peak shifted to a lower frequency side as compared with a peak of single crystal silicon.

88. (Previously Presented) The semiconductor device according to claim 32 wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V{\cdot}sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V{\cdot}sec$ or more.

89. (Previously Presented) The semiconductor device according to claim 31 wherein the crystalline semiconductor islands of the thin film transistors of the pixel portion and the clocked inverter are formed by a same process simultaneously.

90. (Previously Presented) The semiconductor device according to claim 31 wherein a laser Raman spectroscopy of the crystalline semiconductor islands of the thin film transistors of the pixel portion and the clocked inverter exhibits a peak shifted to a lower frequency side as compared with a peak of single crystal silicon.